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Lab 04 Report

ECE 2031 L10

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A diagram of a flowchart

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**Figure 1.** A UML state diagram for a Moore state machine with two inputs (inner & outer) and one output (ajar) and two-bit state encodings. This machine alerts end-users via signal “ajar” when the outer door has been open (logic level 1), and the inner door has been closed (logic level 0) for two clock cycles.

A table of information

Description automatically generated with medium confidence

**Figure 2.** State transition table for state machine defining behaviors of next state logic (Q1+ & Q0+) and output “ajar” for all possible input combinations for each state, both used and unused.

A diagram of a door monitor

Description automatically generated

**Figure 3.** Schematic with pin assignments for the next state logic connected to dual flip flop IC to monitor current state. Inputs “inner”, “outer”, “clock” and “resetn” (active low) and outputs “ajar”. “q1[1]” & “q0[0]” used as outputs to model a next state as a vectorized signal during waveform analysis.

A screenshot of a computer

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**Figure 4.** Simulation of state machine illustrating functional schematic. Inputs “clock” oscillating at 50Hz. Output signal “ajar” only active after two rising-edge clock cycles of “outer” being logic high and “inner” being logic low. State machine resets to state “00” when input “resetn” goes to logic low.

A white circuit board with wires on it

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**Figure 5.** Completed breadboard circuit implementing state machine in actual hardware. Utilizing (left to right) SN74LS04N inverter, SN74HCT00N two-input NAND gate, SN74LS20N four-input NAND gate, and SN74HCT74N dual flip flop. LEDs used as active high to model “Q1” and “Q0” for current state.

A diagram of a door monitor

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**Figure 6.** Schematic with propagation delays for each gate and clock-to-Q delay for flip flop. Worst case delay is 135ns from input “inner” to output “Q1.”